An implant for a visual cortical stimulator

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Abstract - We present the design of an implantable micro-stimulator intended for a cortical visual prosthesis. The device is composed of several integrated modules to be assembled on a thin and flexible substrate providing placement flexibility on the cortex. The stimulator provides the user with significant usage flexibility, supplying biphasic current pulses using either monopolar or bipolar configurations, with single or distributed return electrode, and having a fixed or dynamic reference voltage. Monitoring of electrode-tissue interface condition is possible by measuring both stimulation currents and voltages at any electrode for enhanced safety, and for enabling troubleshooting after implantation. In order to avoid erroneous stimulation to be executed, potentially caused by the implant's wireless transcutaneous power transfer, constant parameters stored in volatile memory are constantly monitored, and in case of data corruption, stimulation is automatically disabled.

A power efficient recovery and regulation circuit is proposed for providing dual supply voltages. Also, a bidirectional wireless link with data rates up to 1.5 Mbps and 500 kbps, downlink and uplink respectively, has been designed for use with a 13.56 MHz carrier. Performances attained with a prototype, combined with the stimulator module's configurable communication protocol, are suitable for a cortical implant having more than 1000 stimulation sites, which is expected to be sufficient for providing blind subjects with a useful vision.

I. INTRODUCTION

ELECTRONIC implants are nowadays used in several biomedical applications, and share many features and basic components. As shown in Fig. 1, chronically implanted wirelessly powered stimulating (recording) devices are composed of a power recovery module, external and internal communication modules for modulating and demodulating data signal encoded over the electromagnetic wave, an output (input) stage, and a central digital controller.

The designer has to take into account the targeted application for decisions concerning the required (tolerated) maximum/minimum currents and voltages of the output (input) stage, the number of channels, the data rate, and so on. Depending on the application, requirements can vary substantially. For example, peripheral nerve stimulators generate a few milliamperes on a very limited number of channels [1-2]. Cochlear implants have similar current requirements, on up to 20 channels [3], and retina implants intend to deliver hundreds of μA to approximately one

Fig. 1. Bloc diagram of a wireless implant.

hundred sites [4-5]. Transfer data rates usually grow according to the number of stimulation sites.

In the specific case of implants designed for restoring functional vision to the blind via intra-cortical stimulation [6-8], subject of the current work, back telemetry (uplink) data rate for occasional monitoring, and the amplitude of stimulation currents for single sites requirements are low, in the range of tens of kHz and μA [9]. On the other hand, the number of stimulation sites/channels is very high. Indeed, for a meaningful image to be perceived by the user, hundreds of stimulation sites are expected to be required [10]. This puts severe constraints on the external to internal (downlink) data rate and the total power efficiency of the device.

This latter consideration is especially important for safety, most probably the prime concern for implants intended for chronic use. As a matter of fact, higher device power consumption not only increases tissue temperature because it dissipates heat, but also implies higher electromagnetic field density through tissues when powering up the device by use of an electromagnetic link.

In addition to keeping device's power consumption to a minimum, features to ensure safe stimulation are desired. Finally, the current stage in research does not allow for deciding on definitive stimulation strategy and optimal parameters. Therefore flexibility is a key issue for today's prototypes.

We will present in the following sections the main modules of an implantable intra-cortical visual stimulator design for which specific optimization effort has been taken regarding issues mentioned above. Section II will give an overview of the design, described in more details in section III. Results from experimental testing of the main modules are presented in section IV, and the main performances will be used to verify if the design is suitable for a prosthesis having more than one thousand stimulation sites.

II. STIMULATOR OVERVIEW

For placement flexibility of the implant over the cortex and minimal pressure on tissues, a thin and modular approach is adopted, as opposed to a monolithic design such as what is presented in [11]. The design comprises several small size stimulation chips (Stimulator Module – SM) lying flat on the cortex, connected to penetrating microelectrode arrays, and a module, placed away from the stimulation sites, interfacing with external components (Interface Module – IM). All components are to be laid out on a common thin flexible substrate, eliminating the need for connectors. Fig. 2 shows a simplified schematic of the device to be implemented from the modules described in the next sections.

The SMs generate constant current biphasic pulses, using monopolar or bipolar configurations. In the case where monopolar stimulation is used, the return current indifferent electrode (*Ref*) can be distant from the stimulation sites, connected to the interface module, or distributed among inactive stimulation microelectrodes.

Communication is ensured by a half-duplex data link using amplitude modulation with On Off Keying (OOK) and Load Shift Keying (LSK) for downlink and uplink, respectively. Low voltages are used both for control and for stimulation. The latter, however, brings the risk of clipping the stimulation pulses if large voltage swing for a particular is required. Since the electrode voltage is usually asymmetrical with respect to the reference electrode, charge imbalance may occur, which in turn may damage tissues permanently [12]. For this reason, considering that electrode-tissue impedance varies with time, and for troubleshooting after implantation, monitoring of any

Fig. 2. Proposed Multi-Module implant.

stimulation site is made available to the user. The voltage to be monitored is buffered from the appropriate SM, and digitization is performed on the IM prior to uplink telemetry. If a SM output current is to be monitored for electrode-tissue interface impedance monitoring, the actual current is monitored through a second return electrode (*MonRef*).

III. DESIGN DESCRIPTION

A. Stimulator Module

A simplified block diagram of the SM is shown in Fig. 3. In the case of the prototype presented in this paper, each SM has four parallel channels, each driving four stimulation microelectrodes (sites). All parameters of stimulation pulses (amplitude – A –, phase duration – D – and interphase duration) are programmable. Pulses frequency, as well as train and inter-train durations, are determined by the rate at which individual pulses are being triggered by the external controller. Electrode shorting can be performed between pulses to ensure charge balance of biphasic pulses.

In order to minimize power consumption, the controller uses a low voltage supply and a configurable communication protocol, minimizing data transfers and its operating clock frequency. To achieve this, every stimulation parameter is sent to the stimulator with a minimal resolution defined in an initial configuration sequence, or is omitted in case a constant parameter can be used. Stimulation on parallel channels can be either sequential (activated upon reception of simulation data) or synchronized. In the latter case, parameters are stored to the appropriate channel controller when received and all stimulations are activated by a subsequent trigger instruction.

Bi-directional current sources are made of complementary thermometer code digital to analog converters, as described in [13], and have four operating ranges (from 17 to 140 μ A).

Stimulation sites are activated through a switch matrix (Fig. 4), which also performs the task of selecting sites for electrode voltage monitoring. The voltage is buffered by a unity gain rail-to-rail amplifier, whose output is connected to a common *Vmon* bus for all SMs.

Because the device is powered via an inductive link, power

Fig. 3. Stimulator Module bloc diagram

Fig. 4. Analog switches controlling the current flowing in stimulation sites j and $j + 1$ on channel i . Grey squares represent electrode.
From Config. Manager decoder

Fig. 5. Configuration parameter corruption detection.

shortage may occur caused by accidental coil movements. In such a case, parameters stored in volatile memory will be corrupted, resulting in every subsequent stimulation to differ from what is expected by the user, leading to hazardous results. To prevent such situation from happening, every configuration parameter is parity encoded prior to be stored, and valid parity of every parameter is continuously verified, as shown in Fig. 5. Upon data corruption detection, stimulation is inhibited, and registers have to be reloaded to continue stimulation normally. Odd parity on an even number of bits is chosen to avoid undetected register set or reset errors.

B. Interface Module

Fig. 6 shows a simplified schematic of the IM, which decodes and transfers stimulation instructions to the appropriate SMs and sends telemetry data to the external user. The IM controller :

- manages half-duplex communication cycles;

- transfers appropriate commands to one or many stimulation modules in a specific or broadcast manner;
- manages monitoring operations and results;
- sets the reference voltage (with respect to the tissue potential);
- manages SM activity to minimize power consumption.

1) Power regulation

For regulating the rectified signal V_{rec} , low drop-out (LDO) linear regulators are used in implantable applications due to their low-noise and small size, as shown in Fig. 7. Regulators using N-type pass devices show fewer stability problems, better regulation and lower ohmic output impedance characteristics than their P-type equivalents.

However, regular N-type pass devices require their gate voltage to be significantly higher than their source output, making the LDO impossible if the feedback amplifier is powered by the input voltage. This would result in reduced power efficiency and stimulating current compliance, limited by the voltage swing of the SMs output stage.

The problem can be eliminated by using a transistor for which the threshold adjustment step is omitted in the fabrication process (native device). These transistors have their V_{th} much lower than regular transistors (typically negative), at the expense of showing larger discrepancies between samples. In the case where the device is used in a negative feedback loop, however, this is not an issue. On the other hand, a regular transistor can be used for the low voltage output since the high regulated voltage provides sufficient voltage swing at the output of the feedback amplifier.

For better power efficiency, a step-down switch capacitor circuit is intended to be used between NMI and MI drains. However, this has not been implemented to date and is part of current work.

The reference voltage required by both regulators, V_{ref} , is set by a bandgap circuit, for which the most important characteristic in the present application is its line rejection. As a matter of fact, temperature does not vary substantially, but the rectified voltage shows strong ripple because a small tank capacitor must be used at the input for size considerations. For

Fig. 6. Interface Module simplified schematic.

Fig. 7. Dual output LDO regulator.

Fig. 8. Start-up and reference circuits for LDO regulator.

this reason, usage of the regulated V_H voltage is preferred over V_{rec} as the bandgap reference's input. However, both the regulator and the reference are then interdependent. So a start-up circuit is used to provide the bandgap reference with the rectified voltage on power up, and then switch to the regulated voltage when the latter becomes sufficient.

The start-up circuit compares V_{rec} and V_H , and feeds the larger of the two to the bandgap reference, as shown in Fig. 78. Transistors $M1-M6$ form two positive feedback loops, modulated by $M1$ and $M3$, and function as a regenerative comparator.

2) Data link

A completely digital demodulator is used for extracting clock and data signals from an OOK modulated 13.56 MHz carrier. Envelope detection is performed by directly digitizing the input carrier using schmitt inverters with different threshold levels (ΔV_{th}), as shown on Fig. 9. An envelope high level results in both inverters toggling at the carrier frequency, while a low level results in constant high outputs. However, because of the gradual decay/rise of the carrier envelope, caused by the channels limited bandwidth and the stored energy in the receiver resonant circuit continuing oscillations when the rectifier cuts off, the inverters will cease their toggling activity for different periods. The output of the narrow ΔV_{th} inverter is used for sampling the state of the wide ΔV_{th} inverter. Also, to minimize the risk of glitches on envelope level transitions, three consecutive samples are used as inputs to a combinatorial logic majority detector.

Most of the power consumption is dissipated by the schmitt inverters, being maximum when the input signal ceases and stabilizes between logic input levels. The inverters are optimized for presenting the largest possible output resistance while allowing their output to toggle at the carrier frequency. With the technology used (0.18 μ m 1.8/3.3V CMOS process), simulations shows that this results in a maximum short-circuit current of 300 μ A.

The digitized carrier and envelope signals are fed to a

Fig. 9. a) Digital demodulator and b) associated waveforms.

Fig. 10. Extracted envelope and data waveforms.

digital clock and data extractor. The carrier is used for generating a data clock at a constant frequency determined by a fixed $f_{Carrier}/f_{Data\ clk}$ ratio. Data modulation uses a constant high period for ones and a short low pulse at the end of the data period for zeros. Envelope low levels reset the carrier counter, which restarts running when the envelope goes back to high. Waveforms associated to data extraction are shown in Fig. 10.

The modulation index of the received signal does not need to be equal to 100% for the large ΔV_{th} to stop toggling, and the period for which the envelope is low is irrelevant for data extraction. Therefore, low pulses can be kept short, allowing for a high duty cycle, highly desirable in ASK modulation since the modulated signal is used for powering the device.

The LSK modulation technique introduced by Tang et al. is used for uploaded telemetry. Turning $M1$ (Fig. 6) on and off changes the rectifier from full-wave bridge to half-wave configurations, hence its equivalent input impedance, resulting in detectable load variations [14].

3) Communication protocol

The implant uses a half-duplex communication protocol. Each cycle is composed of an initializing header, any number of data instructions for the IM or SM (configuration, stimulation, or monitoring), followed by a reply from the implant including monitoring results, and flags that are set in case communication errors were detected in the preceding downlink data stream, or if volatile configuration parameters are corrupted. A stream of ones for 400ms resets the system.

V. SUMMARY

The design and realization of prototypes of the main components of an intra-cortical visual stimulator have been presented. The device offers full latitude on parameters and configurations. Low power is achieved by low voltage of both control and stimulation stage modules, the later being possible especially with dynamic voltage low impedance return current electrode, as well as by the usage of programmable parameters, reducing data and clock rates. Safety features include volatile memory checking, and stimulation voltage monitoring. Measurement on prototype components show that the most stringent performance requirements for a stimulator with 1000 sites are met.

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